5

DIELECTROPHORETIC ARCHITECTURES

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Electric programmability has been the basis for decades of advances in integrated computer component performance. However, once fabricated or assembled, such components—whether blade servers in a data center or microprocessors on a circuit board—are typically stuck in place and require human intervention for reconfiguration, removal, or replacement. For continued advances at the architectural level, mechanical programmability of components may also be needed. One generally promising approach for electromechanical manipulation at the nanoscale and microscale is *dielectrophoresis*, or the net force experienced by a neutral dielectric object in a nonuniform electric field. In this chapter, we review recent advances in dielectrophoretic architectures for computation, focusing particularly on the experimental demonstration of fully reconfigurable nanowire interconnects.

Programmability in electronic systems originates from the ability to form and reform nonvolatile connections. Devices in modern programmable architectures typically derive this ability from controlled internal changes in material composition or charge distribution [1]. However, for "bottom-up" nanoelectronic systems it may be advantageous to derive programmability not only from internal state, but also from the mechanical manipulation of mobile components. Proposed applications that require component mobility include neuromorphic networks of nanostructure-based artificial synapses [2], breadboards for rapid prototyping of nanodevice circuits [3, 4], and fault-tolerant logic in which broken subsystems are replaced automatically from a reservoir [5]. In this chapter, we review recent advances in dielectrophoretic architectures for enabling such computational component mobility, focusing particularly on the experimental demonstration of fully reconfigurable nanowire interconnects—the simplest nanoelectronic components.

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5.1. INTRODUCTION TO DIELECTROPHORESIS

Let us first begin with a discussion of the phenomenon of dielectrophoresis itself. Following Pohl's seminal work on the subject [6], we first calculate the strength of the dielectrophoretic force on a particle and then consider the consequences of dielectrophoresis in media with different electromagnetic responses.

5.1.1. The Dielectrophoretic Effect

Dielectrophoresis is the net force experienced by a dielectric object in a nonuniform electric field. This effect exists because the dipole charges $\pm q$ induced at characteristic locations $r_{\pm}$ are subject to different values of the electric field $E_e(r)$, as shown in Figure 5.1.

There is no net force in a homogeneous electric field, so we can expand,

$$\vec{E}_e(r_+) = \vec{E}_e(r_-) + (\vec{L}\cdot\vec{\nabla})\vec{E}_e(r_-) + \mathrm{O}(L^2).$$

For particles that are small relative to the characteristic length of a field gradient, the net force is given by

$$\vec{F} = \vec{F}_- + \vec{F}_+ = q(\vec{E}_e(\vec{r}_+) - \vec{E}_e(\vec{r}_-)) = (q\vec{L}\cdot\vec{\nabla})\vec{E}_e = (\vec{p}\cdot\vec{\nabla})\vec{E}_e.$$

Under vector transformation,

$$\vec{F} = (\vec{p}\cdot\vec{\nabla})\vec{E}_e = \vec{\nabla}(\vec{p}\cdot\vec{E}_e) - (\vec{E}_e\cdot\vec{\nabla})\vec{p} - \vec{p}\times(\vec{\nabla}\times\vec{E}_e) - \vec{E}_e\times(\vec{\nabla}\times\vec{p}).$$

Since $\vec{\nabla}\times\vec{E}_e = 0$, and for a dielectric that is isotropically, linearly, and homogeneously polarizable, $\vec{p} = v\hat{\alpha}\vec{E}_e$ for body volume v and tensor polarizability $\hat{\alpha}$, the force reduces to

$$\vec{F} = \vec{\nabla}(\vec{p}\cdot\vec{E}_e) - (\vec{E}\cdot\vec{\nabla})\vec{p} = v\hat{\alpha}(\vec{E}_e\cdot\vec{\nabla})\vec{E}_e = \frac{1}{2}v\hat{\alpha}\vec{\nabla}\left|\vec{E}_e\right|^2.$$

Notably, the above dielectrophoretic force is invariant under field inversion.

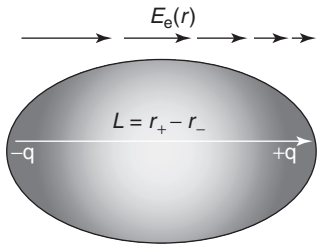

Figure 5.1. Schematic of dielectric particle in inhomogeneous field.

5.1.2. Dielectrophoresis in Media

For a particle with complex dielectric permittivity ε_p^* in a medium ε_m^*, the internal electric displacement is the sum of the particle polarization and the external displacement:

$$\vec{D}_i = \varepsilon_p^* \vec{E}_i = \vec{P} + \varepsilon_m^* \vec{E}_i.$$

Therefore, the polarization scales with the internal electric field as

$$\vec{P} = \left(\varepsilon_p^* - \varepsilon_m^*\right)\vec{E}_i.$$

This polarization generates an additional surface charge dQ on each surface element dF:

$$dQ = \sigma_{pol} \cdot dF = \vec{P} \cdot d\vec{F}.$$

So, applying Coulomb's Law and combining this result with the unperturbed field, we find that

$$\vec{E}_i(\vec{r}_1) = \vec{E}_e(\vec{r}_1) - \oiint \frac{\vec{r}_{12}}{4\pi\varepsilon_m r_{12}^3} dQ_2 = \vec{E}_e(\vec{r}_1) - \oiint \frac{\vec{r}_{12}}{4\pi\varepsilon_m r_{12}^3}\left[\vec{P}(\vec{r}_2) \cdot d\vec{F}_2\right]$$

$$= \vec{E}_e(\vec{r}_1) - \left(\varepsilon_p^* - \varepsilon_m^*\right) \oiint \frac{\vec{r}_{12}}{4\pi\varepsilon_m r_{12}^3}\left[\vec{E}_i(\vec{r}_2) \cdot d\vec{F}_2\right].$$

Since we assumed that the particle is linearly polarizable and, for approximation purposes, considering only the polarization parallel to the electric field, it follows that:

$$\vec{P} = \alpha\vec{E}_e = \left(\varepsilon_p^* - \varepsilon_m^*\right)\vec{E}_i$$

$$\rightarrow \frac{\alpha}{\left(\varepsilon_p^* - \varepsilon_m^*\right)}\vec{E}_e(\vec{r}_1) \cong \vec{E}_e(\vec{r}_1) - \alpha \cdot \mathrm{Proj}_{\vec{\mathrm{E}}_\mathrm{e}(\vec{\mathrm{r}}_1)}\left\{\oiint \frac{\vec{r}_{12}}{4\pi\varepsilon_m^* r_{12}^3}\left[\vec{E}_e(\vec{r}_2) \cdot d\vec{F}_2\right]\right\}$$

$$\rightarrow \frac{\alpha}{\left(\varepsilon_p^* - \varepsilon_m^*\right)}\vec{E}_e(\vec{r}_1) \cong \vec{E}_e(\vec{r}_1) - \frac{\alpha}{4\pi\varepsilon_m^*} \cdot \vec{\mathrm{E}}_\mathrm{e}(\vec{\mathrm{r}}_1) \oiint \frac{\vec{r}_{12} \cdot \vec{\mathrm{E}}_\mathrm{e}(\vec{\mathrm{r}}_1)}{\vec{\mathrm{E}}_\mathrm{e}^2(\vec{\mathrm{r}}_1)}\left[\frac{\vec{E}_e(\vec{r}_2) \cdot d\vec{F}_2}{r_{12}^3}\right]$$

$$\rightarrow \alpha \cong \varepsilon_m^* \cdot \frac{\left(\varepsilon_p^* - \varepsilon_m^*\right)}{\varepsilon_m^* + \frac{\varepsilon_p^* - \varepsilon_m^*}{4\pi} \cdot \oiint \frac{\vec{r}_{12} \cdot \vec{\mathrm{E}}_\mathrm{e}(\vec{\mathrm{r}}_1)}{\vec{\mathrm{E}}_\mathrm{e}^2(\vec{\mathrm{r}}_1)}\left[\frac{\vec{E}_e(\vec{r}_2) \cdot d\vec{F}_2}{r_{12}^3}\right]}$$

The above expression for α/ε_m^* is termed the Clausius–Mossotti factor and is denoted by the frequency-dependent function $K(\omega)$.

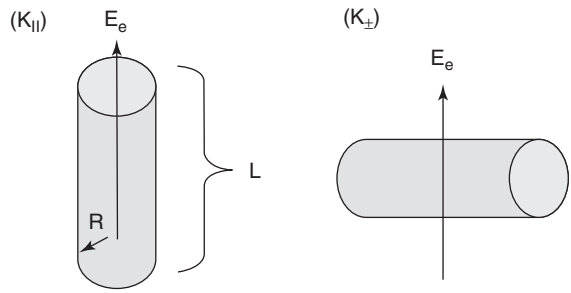

Figure 5.2. Clausius–Mossotti definitions for orientations of a cylindrical particle.

This factor, in both sign and magnitude, is essential to characterizing the dielectrophoretic behavior of a particle in a medium. When the factor is positive, the particle moves toward stronger electric fields; when the factor is negative, the particle moves toward weaker electric fields. For rotationally asymmetric particles, the magnitude can depend strongly on particle orientation relative to the field direction and, in particular, roughly corresponds to the elongation of the particle along the field axis. The nanodevices we focus on in this chapter are cylindrical, so we now present approximate Clausius-Mossotti expressions for cylindrical particles parallel and perpendicular to a field, as shown in Figure 5.2:

$$K_{\|}(f) \cong \frac{\varepsilon_p^* - \varepsilon_m^*}{\varepsilon_m^* + (\varepsilon_p^* - \varepsilon_m^*)(1 - (1 + R^2/L^2)^{-1/2})}$$

and

$$K_{\perp}(f) = \frac{\varepsilon_p^* - \varepsilon_m^*}{\varepsilon_m^*\left(1 - \frac{\pi}{8}\right) + \varepsilon_p^*\left(\frac{\pi}{8}\right)} \sim 3\frac{\varepsilon_p^* - \varepsilon_m^*}{\varepsilon_p^* + 2\varepsilon_m^*}.$$

5.2. DIELECTROPHORETIC ASSEMBLY AND TRANSPORT OF NANODEVICES

Having completed our discussion of the theory of dielectrophoresis, we are now ready to explore its practical applications to nanocomputation. Let us first consider the problem of assembling individual nanodevices. Various approaches for manipulating electronic nanostructures have been developed, including mechanical [7], optical [8, 9], electrostatic [10, 11], and dielectrophoretic [6] methods. Dielectrophoresis is particularly attractive for inexpensive and massively parallel manipulation [12] of neutral microscale and nanoscale objects using only standard semiconductor fabrication technologies. It has been used to trap a variety of structures from suspensions, including NiSi nanowires [13], CdS nanowires [14], GaN nanowires [15], carbon nanotubes [16], silicon microblocks [17], ZnO

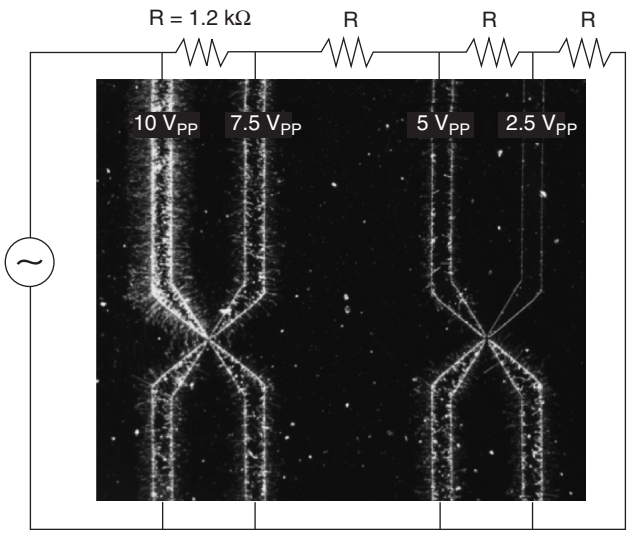

Figure 5.3. Dark-field microscope image demonstrating the trapping of large numbers of nanostructures, which are visible as lines perpendicular to the electrode faces, at relatively low voltages.

nanorods and nanobelts [18, 19], and gold nanowires [20]. An example of the ability of dielectrophoresis to trap nanostructures with relatively low voltages is shown in Figure 5.3. Previous electrical transport measurements of dielectrophoretically trapped structures have been performed either after immobilizing the structures through drying [15–19] or chemical binding [20], or performed over large films of parallel interconnects [16]. In this work we demonstrate for the first time that dielectrophoresis may also be used to reconfigure and disassemble nanowire interconnects and that our process is compatible with the assembly and electronic characterization of individual nanowire devices.

5.3. DIELECTROPHORETIC RECONFIGURATION OF NANODEVICES

Assembly of nanodevices is itself worthy of scientific interest, but the beauty of dielectrophoretic architectures lies in their versatility, since they enable not just the assembly but the reconfiguration of nanodevices as well. We now proceed to discussion of the recent experimental demonstration of reconfigurable nanowire interconnects [21], which exemplifies that versatility.

5.3.1. Fabrication of a Nanowire Trapping Architecture

For interconnects, p-type silicon nanowires were grown by the vapor-liquid-solid method [22], using 20-nm Au nanocluster catalysts (Ted Pella), and SiH_4 reactant

(99.7%) and B_2H_6 dopant (0.3%) in He carrier gas (100 ppm) at 450 torr and 450 °C. Growth was performed for 10–60 min to achieve nanowire lengths of 10–60 μm. The nanowire growth wafer was sonicated lightly in isopropanol for 1 min. The suspension was vacuum filtered using a 12-μm mesh (Millipore Isopore) in order to remove unnucleated Au catalyst particles and short nanowires. The filter mesh was sonicated in isopropanol, and the suspension was again filtered. The second filter mesh was sonicated in benzyl alcohol for 2 min and the suspension was used for trapping experiments. Benzyl alcohol was selected as a viscous, low-vapor-pressure solvent [23] for reconfiguration in order to damp Brownian motion, minimize toxicity [24], and allow ambient operation. Additionally, its static relative permittivity is slightly smaller than that of bulk Si (11.9 versus 12.1, respectively) [23], reducing van der Waals interactions at low frequencies and favouring dielectrophoretic trapping of conductive structures [6]. Heavily doped silicon nanowires were selected as interconnects to demonstrate potential compatibility of our technique with the assembly of more complex semiconducting nanostructures, such as axial heterostructures [25].

Trapping experiments were performed with 100-nm Au electrodes (5 nm Cr wetting layer) to avoid oxidative damage, on a Si wafer with a 200-nm oxide to prevent shorts. Thicker electrodes, with reduced fringing fields, were found to better allow nanowires to migrate along their edges toward the trapping region. Thinner electrodes tended to permanently pin nanowires to the top electrode faces wherever they were first trapped. The electrodes were defined by e-beam lithography with a 10° taper angle and a 1-μm tip radius of curvature.

The nanowire suspension was pipetted onto the electrode chip to form a 250-μm-thick reservoir, as shown schematically in Figure 5.4a. For trapping, electrode pairs were biased at 10 kHz to minimize both solvent electrolysis and parasitic capacitance. The bias was modulated into 10-ms bursts at 110 V_{RMS} with a period of 100 ms, which allowed migration of nanowires toward the trapping region in controlled steps. The time between bursts was manually increased to 1000 ms as nanowires approached the inter-electrode region, and the bursts were halted when the desired number of nanowires had been trapped. Movies of nanowire motion were recorded at 4 fps.

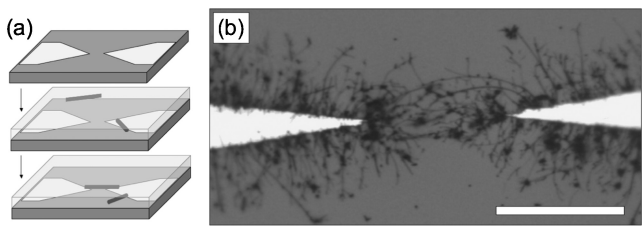

Figure 5.4. Dielectrophoretically trapped nanowires. (a) Schematic illustration of nanowire trapping process. (b) Light microscope image of multiple nanowires stably trapped between electrodes separated by 40 μm. Scale bar is 40 μm.

Electrical characterization was performed by manually switching the electrodes from the trapping voltage source to a measurement apparatus (Agilent 4156C). A 10-V sawtooth bias at 10 Hz was used and the measured currents were binned by voltage and averaged to remove hysteresis. Nanowire movement in the plane of the chip during transport measurement was minimal, since transport voltages were an order of magnitude smaller than trapping voltages.

5.3.2. Trapping Nanowire Interconnects

Nanowires up to 55 μm in length were stably trapped, as shown in Figure 5.4b, with noticeable bending due to the trapping field inhomogeneity. The longest previously reported one-dimensional nanostructures to be trapped by dielectrophoresis at both ends were less than 15 μm long and showed minimal bending [14].

For larger electrode gaps, nanowires at either tip appeared not to experience significant bending toward the opposite electrode, while shorter gaps caused significant accumulations of wires, as shown in Figure 5.5.

Confirmation that the trapping voltage was not substantially attenuated was provided by observation of a single scattering fringe around the electrodes in dark-field mode, as shown in Figure 5.6, which was consistent with the DC Kerr effect [6] at 155-V peak bias across a 10-μm gap.

The burst method was also delicate enough to enable trapping of individual nanowires when the reservoir was diluted below 2×10^{-13} M, as shown in Figure 5.7a. Before nanowire interconnects were assembled, DC transport between electrode pairs was nearly ohmic, as shown in Figure 5.7b. The measured current of 0.3 μA at 1-V bias and 40-V/s sweep rate was consistent with electrooxidation of benzyl alcohol [26, 27] at 1-μm-radius electrode tips.

However, after a 50-μm-long nanowire was trapped, the conductance became nonlinear and showed a 50% enhancement at 10-V bias, as shown in Figure 5.7c. Treating the device as an electrooxidative resistance in parallel with a series nanowire resistance and Schottky contacts [28], a nanowire transport curve was calculated, as shown in Figure 5.7d. The nanowire exhibited a calculated linear

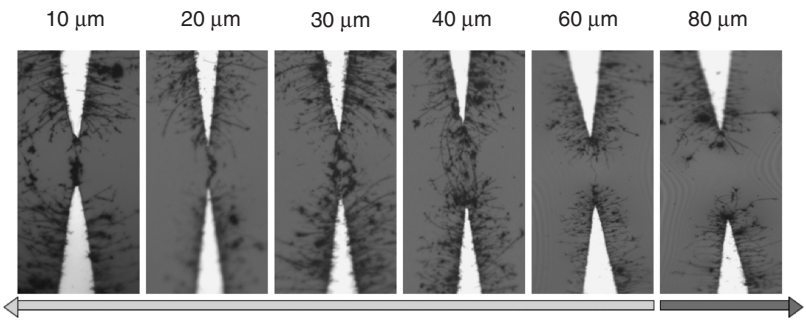

Figure 5.5. Nanowires trapped by electrodes separated by various distances.

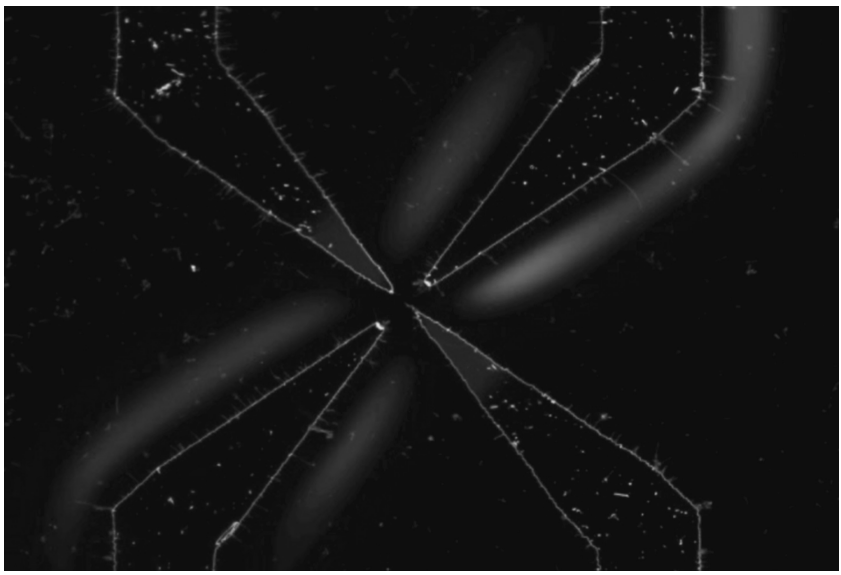

Figure 5.6. Scattering fringes about active electrodes as viewed in dark-field mode, attributed to the DC Kerr effect.

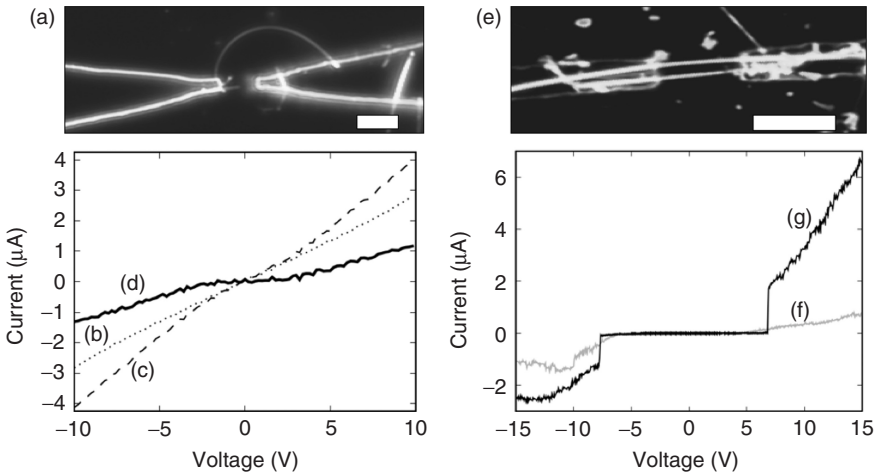

Figure 5.7. Electrical transport in trapped nanowires. (a) Dark-field microscope image of a single nanowire trapped by an electrode pair under solvent with electrical transport (b) measured with solvent, (c) measured with trapped nanowire in solvent, and (d) calculated for nanowire alone. (e) Dark-field microscope image of two trapped nanowires on dried substrate with electrical transport measured (f) immediately after drying and (g) after several voltage sweeps. Scale bars are 10 μm.

response resistivity of $3.8 \times 10^{-3}\,\Omega \cdot$ cm (6.0-MΩ resistance), consistent with a B doping ratio of 2000:1, and an estimated barrier potential of 2.0 V. The barrier potential was higher than the 0.34 V measured in evaporated Au/p-Si junctions [29], and is attributed to incomplete contact of the nanowire with the electrodes.

Further confirmation that dielectrophoretically trapped nanowires acted as interconnects was provided by substituting ethanol as a solvent and permitting the substrate to dry after trapping. A pair of nanowires thus trapped, as shown in Figure 5.7e, appeared to rest on both electrode faces but initial voltage sweeps yielded a 30-MΩ resistance, as shown in Figure 5.7f. After several sweeps, however, a sharp current turn-on was observed at 6.8–7.8 V, as shown in Figure 5.7g, which may indicate electrostatically induced bending of the nanowires to better contact the electrodes. Above the turn-on bias, the nanowires exhibited a 1.7-MΩ combined resistance, which is compatible with the solvent-based result.

5.3.3. Reconfiguring Nanowire Interconnects

The reported method for trapping nanowire interconnects furthermore enabled reconfiguration, since nanowires were maximally polarized when aligned between a pair of electrode tips. Reconfiguration of a nanowire bundle was achieved using "source" and "drain" electrodes with opposite phase and a "latch" electrode with variable phase. Several nanowires were independently trapped between the source and latch electrodes with 100-ms-period bursts, as shown in Figure 5.8a, and then bundled with 250-ms-period bursts, as shown in Figure 5.8b. The phase of the latch electrode was then inverted, with the same burst period, causing the nanowire bundle to experience a dielectrophoretic force toward the drain electrode. Because the electrode tips were arranged in an isosceles right triangle formation, the torque about the latch electrode was higher than that about the source electrode, and the nanowire remained in contact with the latch electrode during the motion, as shown in Figure 5.8c. The reconfiguration was completed 0.25–0.75 s after the phase inversion, as shown in Figure 5.8d, and could be reversed by restoring the original phase of the latch electrode, as shown in Figure 5.8e.

Similarly, parallel reconfiguration of a pair of nanowire interconnects was achieved with four electrodes in a 10-μm square, as shown in Figure 5.9. To accomplish this, the relative phases between diagonally opposite electrodes were fixed and the relative phase of the diagonal pairs was inverted. Dielectric breakdown of some nanowires occurred and short fragments were visible around the connecting nanowires.

For theoretical comparison, we now calculate how rapidly a nanowire might be dielectrophoretically reconfigured. The dielectrophoretic force per unit length on a cylindrical nanowire with length l_{wire} and diameter d_{wire} is given by

$$F_{dep} = \frac{1}{8}\varepsilon_{solv}\pi d_{wire}^2 \mathrm{Re}\left\{\vec{K}(f)\cdot\vec{\nabla}(\vec{E}^2)\right\}\,\hat{\nabla}(\vec{E}^2)$$

where ε_{solv} is the solvent permittivity and $\vec{K}(f)$ is the frequency-dependent Clausius–Mossotti factor [6].

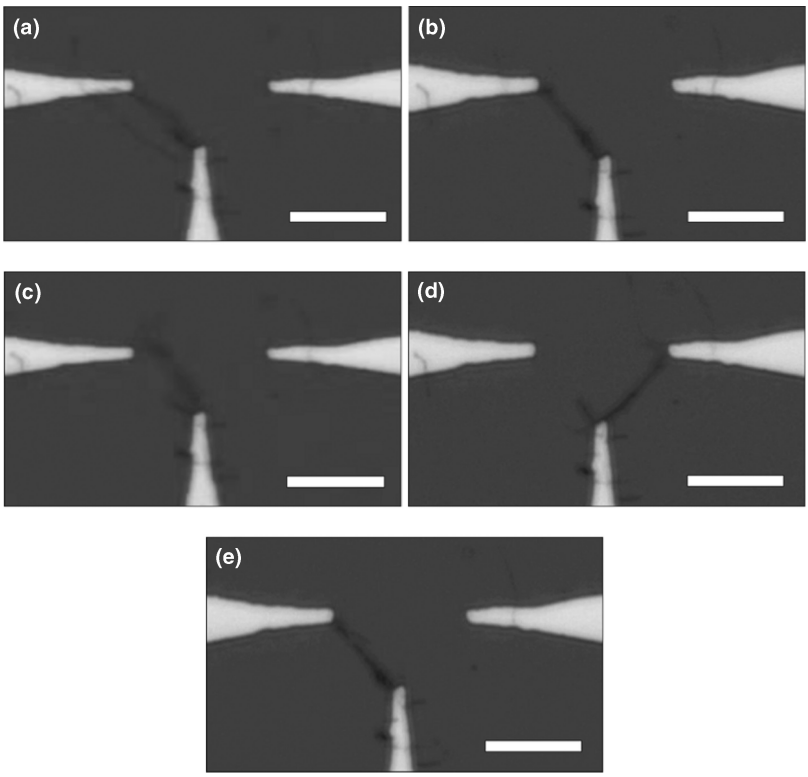

Figure 5.8. Microscope images of 3-electrode serial reconfiguration of nanowires. The relative phase between the left (source) and middle (latch) electrodes is modulated from (a,b) 180° to (c,d) 0° to (e) 180°. Scale bars are 15 μm.

For $l_{wire} >> d_{wire}$, the Clausius–Mossotti component perpendicular to the nanowire axis is approximately

$$K_{\perp} = \frac{\tilde{\varepsilon}_{wire} - \tilde{\varepsilon}_{solv}}{\tilde{\varepsilon}_{solv}\left(1 - \frac{\pi}{8}\right) + \tilde{\varepsilon}_{wire}\left(\frac{\pi}{8}\right)},$$

where $\tilde{\varepsilon}_X \equiv \varepsilon_X - i\sigma_X/(2\pi f)$ are the complex permittivities of nanowire and solvent (the solvent is assumed to be nonconductive at trapping frequencies). Approximating the gradient of the field energy density in the inter-electrode space as uniform, $\nabla(\vec{E}^2)\tilde{V}_{sd}^2/L^3$, where L is the distance between electrode tips.

The dielectrophoretic force is opposed by Stokes drag. The drag coefficient for an infinitely long, cylindrical nanowire [30] is given by

$$C_D \equiv \frac{F_{drag}}{\frac{1}{2}\rho_{wire}u^2 d} \approx \frac{8\pi}{\mathrm{Re}(2.002 - \ln \mathrm{Re})},$$

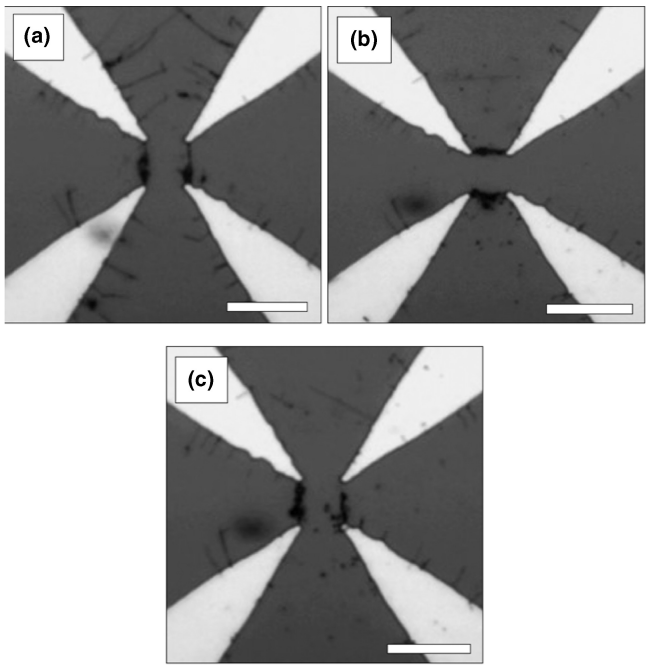

Figure 5.9. Microscope images of 4-electrode parallel reconfiguration of nanowires. Each pair of diagonally opposite electrodes is held at a constant relative phase of 180°, while the relative phase between the upper-left and upper-right electrodes is modulated from (a) 0° to (b) 180° to (c) 0°. Scale bars are 20 μm.

where F_{drag} is the drag force per unit length, ρ_{wire} is the nanowire density, u is the nanowire velocity, and $Re \sim d\rho_{solv}u/\mu$ is the Reynolds number for solvent density ρ_{solv} and dynamic viscosity μ. Assuming bulk mechanical properties of silicon and benzyl alcohol [23] and matching drag and dielectrophoretic forces, the terminal velocity during switching perpendicular to the nanowire axis is calculated to be $u_{\perp} \approx 30\,\mu m/s$, implying a 0.3-s reconfiguration time. This time is consistent with the serial reconfigurations observed, validating our model.

5.3.4. Disassembling Nanowire Interconnects

Finally, it should be mentioned that electrically driven nanowire disassembly was also found to occur. In an example of this effect, a single nanowire that was initially trapped on one electrode, as shown in Figure 5.10a, was pulled into the inter-electrode region and a gas bubble immediately formed there, as shown in Figure 5.10b. After the bubble dispersed, only short nanowire fragments remained, as shown in Figure 5.10c. This effect was observed for about 1/3 of

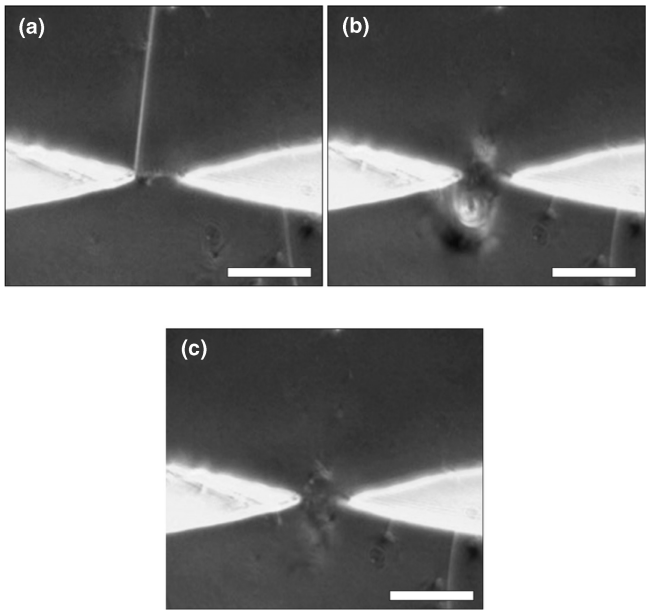

Figure 5.10. Disassembly of nanowire interconnects by thermal detonation. (a) Stably trapped nanowire before detonating voltage pulse. (b) Vapor bubble resulting from thermal detonation. (c) Only submicron fragments remain. Scale bars are 20 μm.

the nanowires trapped in inter-electrode regions and might be explained by variation in the nanowire conductivities and/or the formation of exceptionally good contacts, which could lead to current densities as high as $5 \times 10^{10}\,\mathrm{A \cdot m^{-2}}$ and thermal detonation. After the original nanowires were destroyed, the inter-electrode regions were typically able to trap new interconnects, so this effect might prove useful in fault-tolerant applications for severing connections to non-functioning components.

5.3.5. Summary of Implementation

The first assembly, reconfiguration, and disassembly of nanowire interconnects through dielectrophoresis has been presented. Silicon nanowires up to 55 μm long were trapped, and solvent-based transport studies show a 50% conductivity enhancement in the presence of the nanowires. Once assembled, these nanowire interconnects could then be reconfigured and disassembled using periodic voltage bursts. These results open up the possibility of colloidal, nanostructured connection architectures for computation.

5.4. LARGER-SCALE ARCHITECTURES

With our discussion of individual component reconfigurability concluded, we now advance to an exploration of the feasibility of larger-scale dielectrophoretic architectures. For dielectrophoresis to find real-world applications to nanocomputation, logic—at least at the gate level—must be demonstrated.

5.4.1. 1 × 1 Crossed Interconnects

In Section 5.3 we experimentally demonstrated the reconfiguration of interconnects geometrically occupying single sides or pairs of sides of a square. As a next step toward larger-scale architectures, we should also consider interconnects that do not lie on the circumference of the trapping region, but instead span it. In particular, we may estimate the value of the term ∇E^2, which is crucial to the dielectrophoretic strength, for either type of configuration, as shown schematically in Figure 5.11.

Recall that we may approximate the trapping force by assuming a uniform electric field gradient near the energy minimum. Therefore, for the geometry shown in Figure 5.11, for the noncircumferential interconnect (I),

$$\nabla E^2 \sim (V)^2/(d\sqrt{2})^3 = \frac{1}{2^{3/2}} \cdot \frac{V^2}{d^3},$$

and for the circumferential interconnect (II),

$$\nabla E^2 \sim (V/2)^2/(d)^3 = \frac{1}{2^2} \cdot \frac{V^2}{d^3}.$$

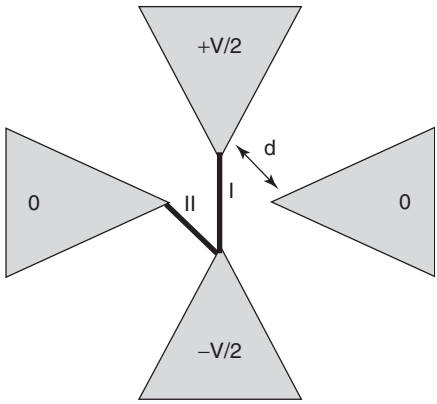

Figure 5.11. Schematic diagram for circumferential (II) versus noncircumferential (I) interconnects in a 1 × 1 crossbar.

Since the value is larger for the noncircumferential case, stable trapping of diagonal interconnects should be possible. (There is suggestive experimental data that stable diagonal interconnects can indeed be achieved [14], although the substrate in that case was dried before imaging.) Moreover, since $K_{\perp} \ll K_{||}$, a short field burst perpendicular to an existing wire should not disrupt it.

5.4.2. 2 × 2 Crossbar

We can perform a similar, albeit more entailed, analysis to determine the feasibility of stable noncircumferential interconnects in larger crossbars, such as the 2×2 geometry we now consider.

For the specific octagonal electrode tip geometry and voltages shown in Figure 5.12, we can calculate all force values ($F \equiv \nabla E^2$):

$$\frac{F_2}{F_1} = \frac{\left(\frac{1}{2} - a\right)^2}{\left[\frac{1}{\sqrt{2}}(1-p)\right]^3}. \quad \frac{F_3}{F_1} = \frac{(2a)^2}{p^3}, \quad \frac{F_4}{F_1} = \frac{\left(\frac{1}{2} + a\right)^2}{\left[\sqrt{\frac{1}{2} + \frac{p^2}{2}}\right]^3},$$

$$\frac{F_4}{F_1} = \frac{\left(\frac{1}{2} + a\right)^2}{\left[\sqrt{\frac{1}{2} + \frac{p^2}{2}}\right]^3}, \qquad \frac{F_5}{F_1} = \frac{(2a)^2}{\left[\sqrt{p^2+1}\right]^3},$$

In order to estimate the proper conditions for trapping of non-circumferential interconnects, particularly the interconnect at F_1, we are most interested in the

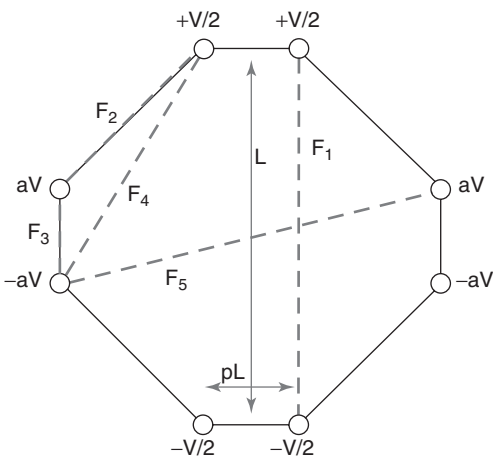

Figure 5.12. Schematic diagram for dielectrophoretic force constants for various interconnects in a 2×2 crossbar geometry. Circles indicate electrode tips.

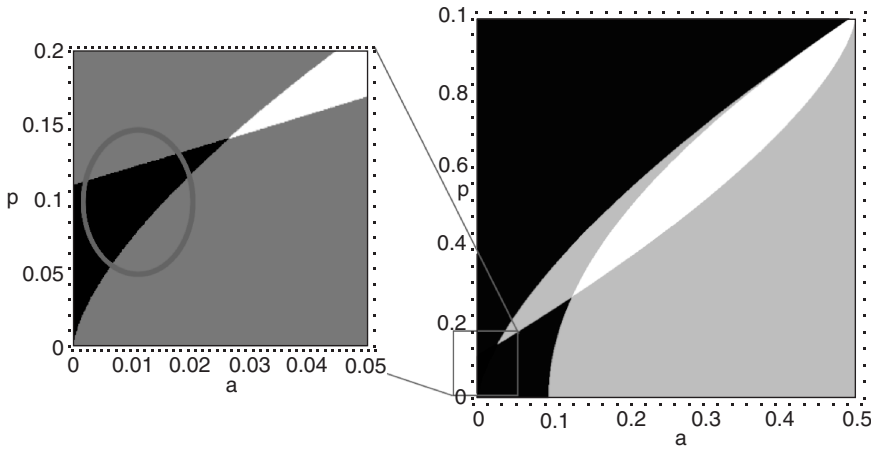

Figure 5.13. Phase diagram of dielectrophoretic forces (F_2, F_3, F_4, F_5)/F_1 in the space of dimensionless electrode voltages (a) versus electrode spacings (p) in a 2×2 crossbar geometry. Darker regions indicate that more of F_2, F_3, F_4, F_5 are less than F_1.

parameters $0 < a < 1/2$, $0 < p < 1$ that cause all of these ratios to fall below 1. We survey this phase space in Figure 5.13, and find that—at least by this prediction method—long crossbar-style interconnects should be possible as long as the parallel electrode pitch is 10–20 times smaller than the interconnect length ($0.05 < p < 0.1$) and electrodes uninvolved in the trapping are kept grounded ($a = 0$).

5.4.3. Field-Programmable Gates

In addition to interconnect architectures, it should also be possible to more directly build logic based on dielectrophoretic reconfiguration of nanodevices. In particular, with the proper arrangement of pairs of the latching electrodes shown in Figure 5.8, digital logic gates can be reproduced. In these gates, as depicted in Figure 5.14, the relative phase of two electrodes determines the position of interconnects which can then carry or block a current path specific to the logical operation required.

5.4.4. Packaging

In order to enable the vision of dielectrophoretic architectures for self-repairing computer components, development of stable colloidal reservoirs of components will be crucial. Fortunately, many dielectric solvents, such as the benzyl alcohol used in the reconfigurable nanowire work discussed above, have low vapor pressures. This property may enable colloidal reservoirs of replacement components to be stably sealed into a chip carrier package, as shown in Figure 5.15.

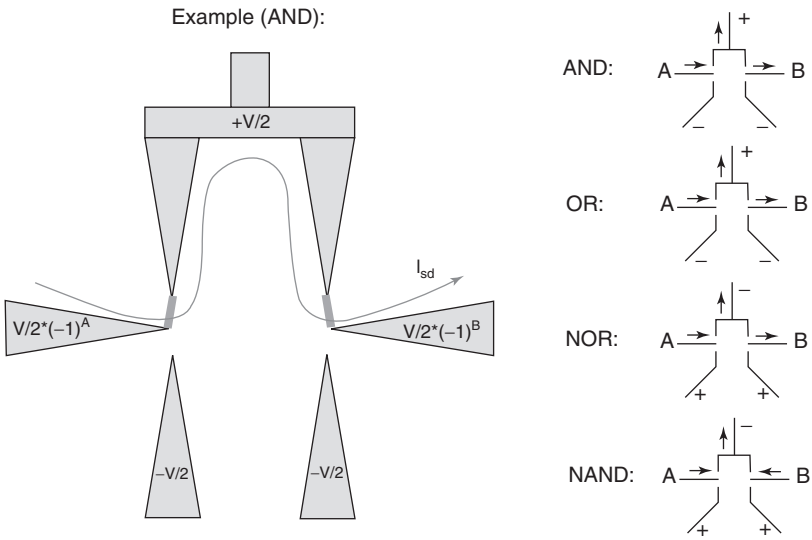

Figure 5.14. Field programmable gates in which short voltage pulses on two electrodes serve as input (phase indicated by sign), and current indicated by arrows serves as output.

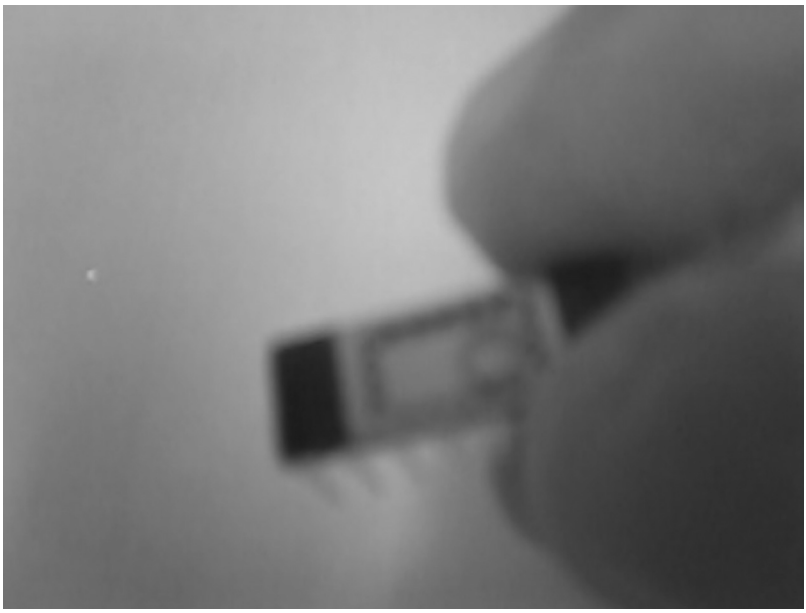

Figure 5.15. Packaged nanowire reservoir.

In preliminary tests, sealed reservoirs of benzyl alcohol for dielectrophoretic manipulation remained stable, in the sense that nanowires remained suspended and there was no visible leakage of solvent, for more than a week under refrigeration.

5.5. CONCLUSIONS

We have reviewed recent progress toward the development of dielectrophoretic architectures for integrated nanoelectronic computation. Focusing on the demonstration of reconfigurable nanowire interconnects, we also derived general strategies for scaling, integrating, and packaging such dielectrophoretic systems.

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